**IN THE SPECIFICATION**

Please replace the paragraph starting on page 4, line 3 with the following paragraph:

FIG. 3 is a graph of a probability density function for Gaussian distributed phase error having a standard deviation of 0.2 used with the present invention;

Please replace the paragraph starting on page 4, line 5 with the following paragraph:

FIG. 4 is a coarse histogram with spacing of T/4 for the distribution of FIG. 3 used with the present invention;

Please replace the paragraph starting on page 13, line 10 with the following paragraph:

FIG. [4]5 shows an outline block diagram of an apparatus 10 having a phase error window block 11, a pair of counters 12 and 13, a comparator 14, a register 15, and a memory 16 having a look-up table stored therein. The phase error window block 11 receives four clock inputs, which are in quadrature with each other, labelled CLK0, CLK90, CLK180 and CLK270 and a data edge pulse. The phase error window block 11 determines which phase window the phase error falls into and provides signals which update the counters 12 and 13. The first (N-bit) counter 12 records the number of phase errors falling into the windows - ¼ d $\Delta T$ < 0 and 0 d $\Delta T$ < ¼ (e.g.

n2+n3) and the second (M-bit) counter 13 records the number of phase errors falling into the windows - ½ d ΔT < - ¼ and ¼ d ΔT < ½ (e.g. n1+n4). The comparator 13 is used to determine when the first counter 12 reaches a limit of $2^N - 1$. When this occurs, the value in the second counter 13 is latched into the register 15 and both counters 12 and 13 are reset for the process to be repeated. The latched value in register 15 is then used to estimate A2+A3 as:

$$A2 + A3 \approx \frac{n2 + n3}{n1 + n2 + n3 + n4} = \frac{2^n - 1}{2^n - 1 + n1 + n4} \qquad (7)$$